ESE-2005 Assignment 3 Logic Gate

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Exercise

1. Draw the symbol, Boolean equation, and truth table for

(a) a three-input OR gate.

\*Truth table: -

A

B Y

C

\*Boolean equation: -

Y= A+B+C

\*Truth Table: -

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | A | B | C | Y |
| A’ B’ C’ | 0 | 0 | 0 | 0 |
| A’ B’ C | 0 | 0 | 1 | 1 |
| A’ B C’ | 0 | 1 | 0 | 1 |
| A’ B C | 0 | 1 | 1 | 1 |
| A B’ C’ | 1 | 0 | 0 | 1 |
| A B’ C | 1 | 0 | 1 | 1 |
| A B C’ | 1 | 1 | 0 | 1 |
| A B C | 1 | 1 | 1 | 1 |

(b) a three-input exclusive OR (XOR) gate.

\*Truth table: -

A

B Y

C

\*Boolean equation: -

Y= A \oplus B \oplus C = ABC + A’B’C + A’BC’ + AB’C’

\*Truth Table: -

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | A | B | C | Y |
| A’ B’ C’ | 0 | 0 | 0 | 0 |
| A’ B’ C | 0 | 0 | 1 | 1 |
| A’ B C’ | 0 | 1 | 0 | 1 |
| A’ B C | 0 | 1 | 1 | 0 |
| A B’ C’ | 1 | 0 | 0 | 1 |
| A B’ C | 1 | 0 | 1 | 0 |
| A B C’ | 1 | 1 | 0 | 0 |
| A B C | 1 | 1 | 1 | 1 |

(c) a four-input XNOR gate.

\*Truth table: -

A

B

Y

C

D

\*Boolean equation: -

Y= A   B C D

\*Truth Table: -

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | A | B | C | D | Y |
| A’B’C’D’ | 0 | 0 | 0 | 0 | 1 |
| A’B’C’D | 0 | 0 | 0 | 1 | 0 |
| A’B’C D’ | 0 | 0 | 1 | 0 | 0 |
| A’B’C D | 0 | 0 | 1 | 1 | 1 |
| A’B C’D’ | 0 | 1 | 0 | 0 | 0 |
| A’B C’D | 0 | 1 | 0 | 1 | 1 |
| A’B C D’ | 0 | 1 | 1 | 0 | 1 |
| A’B C D | 0 | 1 | 1 | 1 | 0 |
| A B’C’D’ | 1 | 0 | 0 | 0 | 0 |
| A B’C’D | 1 | 0 | 0 | 1 | 1 |
| A B’C D’ | 1 | 0 | 1 | 0 | 1 |
| A B’C D | 1 | 0 | 1 | 1 | 0 |
| A B C’D’ | 1 | 1 | 0 | 0 | 1 |
| A B C’D | 1 | 1 | 0 | 1 | 0 |
| A B C D’ | 1 | 1 | 1 | 0 | 0 |
| A B C D | 1 | 1 | 1 | 1 | 1 |

2. A three-input AND-OR (AO) gate shown in Figure 1.42 produces a TRUE

output if both A and B are TRUE, or if C is TRUE. Complete a truth

table for the gate.

Y= A.B + C

Truth Table: -

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | A | B | C | A.B | Y=A.B + C |
| A’B’C’ | 0 | 0 | 0 | 0 | 0 |
| A’B’C | 0 | 0 | 1 | 0 | 1 |
| A B’C | 0 | 1 | 0 | 0 | 0 |
| A’B C | 0 | 1 | 1 | 0 | 1 |
| A B’C’ | 1 | 0 | 0 | 0 | 0 |
| A B’C | 1 | 0 | 1 | 0 | 1 |
| A B C’ | 1 | 1 | 0 | 1 | 1 |
| A B C | 1 | 1 | 1 | 1 | 1 |

3. A three-input OR-AND-INVERT (OAI) gate shown below produces a FALSE input if C is TRUE and A or B is TRUE. Otherwise it produces a TRUE output. Complete a truth table for the gate.

Y= [(A+B).C]’

Truth Table: -

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | A | B | C | A+B | (A+B)C | Y=[(A+B).C]’ |
| A’B’C’ | 0 | 0 | 0 | 0 | 0 | 1 |
| A’B’C | 0 | 0 | 1 | 0 | 0 | 1 |
| A B’C | 0 | 1 | 0 | 1 | 0 | 1 |
| A’B C | 0 | 1 | 1 | 1 | 0 | 1 |
| A B’C’ | 1 | 0 | 0 | 1 | 0 | 1 |
| A B’C | 1 | 0 | 1 | 1 | 1 | 0 |
| A B C’ | 1 | 1 | 0 | 1 | 0 | 1 |
| A B C | 1 | 1 | 1 | 1 | 1 | 0 |

4. Is it possible to assign logic levels so that a device with the transfer characteristics shown below would serve as an inverter? If so, what are the input and output low and high levels (VIL, VOL, VIH, and VOH) and noise margins (NML and NMH)? If not, explain why not.

A screenshot of a cell phone

Description automatically generated



Vil=2.5v Voh=4v

Vih=3v Vol=1.5v

Nl=2.5-1.5= 1v

Nh=4v-3v= 1v

This transfer function can act as a inverter.

5. Is it possible to assign logic levels so that a device with the transfer characteristics shown below would serve as an inverter? If so, what are the input and output low and high levels (VIL, VOL, VIH, and VOH) and noise margins (NML and NMH)? If not, explain why not.

A screenshot of a cell phone

Description automatically generated



Vil=1v Voh=3.5v

Vih=3.5v Vol=1v

Nl=1-1= 0v

Nh=3.5v-3.5v= 0v

6. Is it possible to assign logic levels so that a device with the transfer characteristics shown below would serve as an buffer? If so, what are the input and output low and high levels (VIL, VOL, VIH, and VOH) and noise margins (NML and NMH)? If not, explain why not.

A screenshot of a cell phone

Description automatically generated



Vil=2v Voh=4.5v

Vih=4v Vol=1v

Nl=2v-1v= 1v

Nh=4.5v-4v= 0.5v

The transfer characteristics act as a buffer.

7. Ben Bitdiddle has invented a circuit with the transfer characteristics shown below that he would like to use as a buffer. Will it work? Why or why not? He would like to advertise that it is compatible with LVCMOS and LVTTL logic. Can Ben’s buffer correctly receive inputs from those logic families? Can its output properly drive those logic families? Explain.

A screenshot of a cell phone

Description automatically generated



Vil=1.2v Voh=3.0v

Vih=1.8v Vol=1.0v

Nl=1.2v-1v= 0.2v

Nh=3v-4v= 1.8v

8. While walking down a dark alley, Ben Bitdiddle encounters a two input gate with the transfer function shown below. The inputs are A and B and the output is Y. What kind of logic gate did he find? What are the approximate high and low logic levels?

A picture containing drawing

Description automatically generated

This transfer chacteristics is for 2 input AND gate because output is high when both the inputs are high.

A and B are inputs and Y is the output.

Vil=2v Voh=3v

Vih=3v Vol=2.5v